

Z10PE-D8 WS Repair Guide

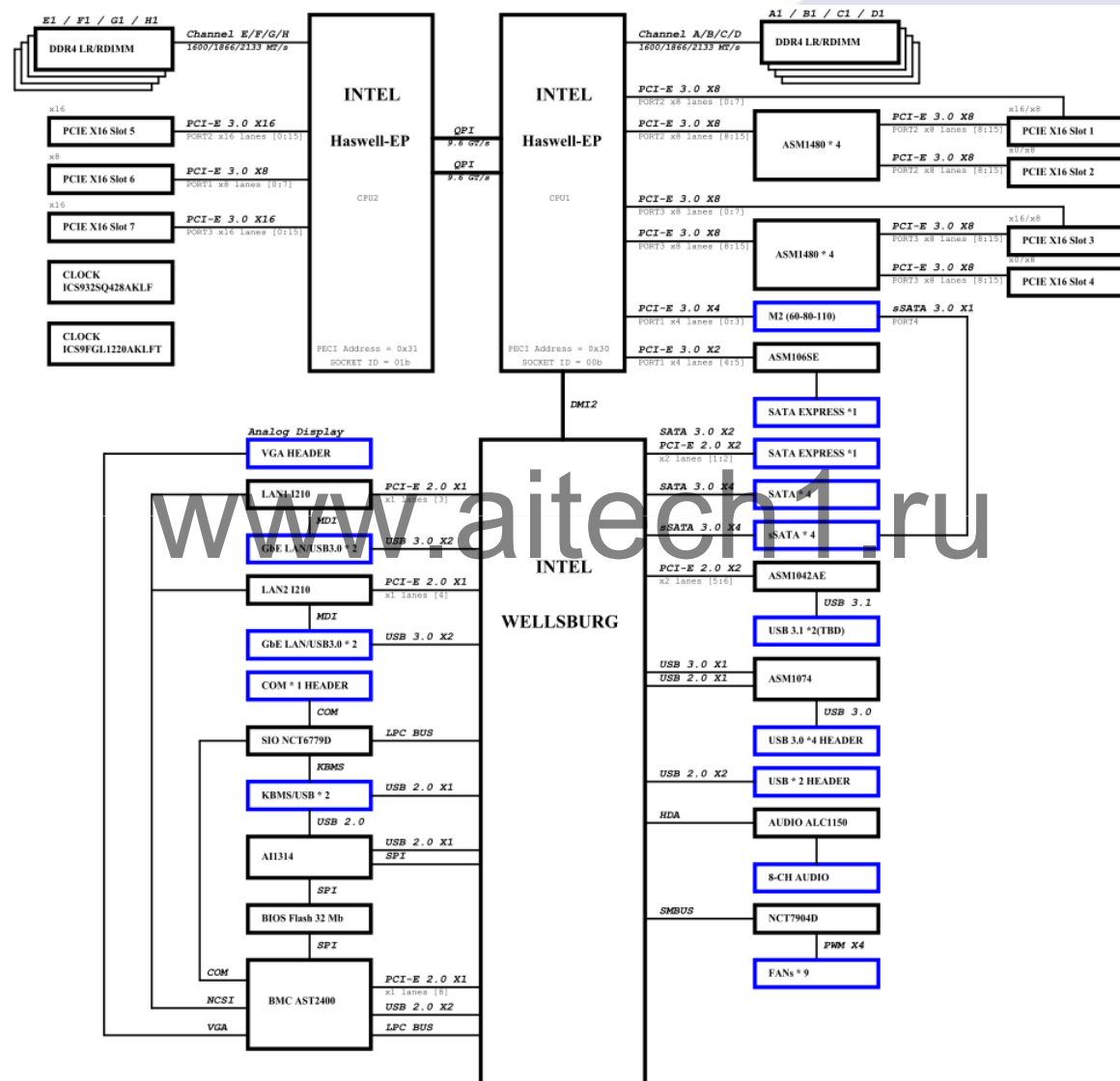
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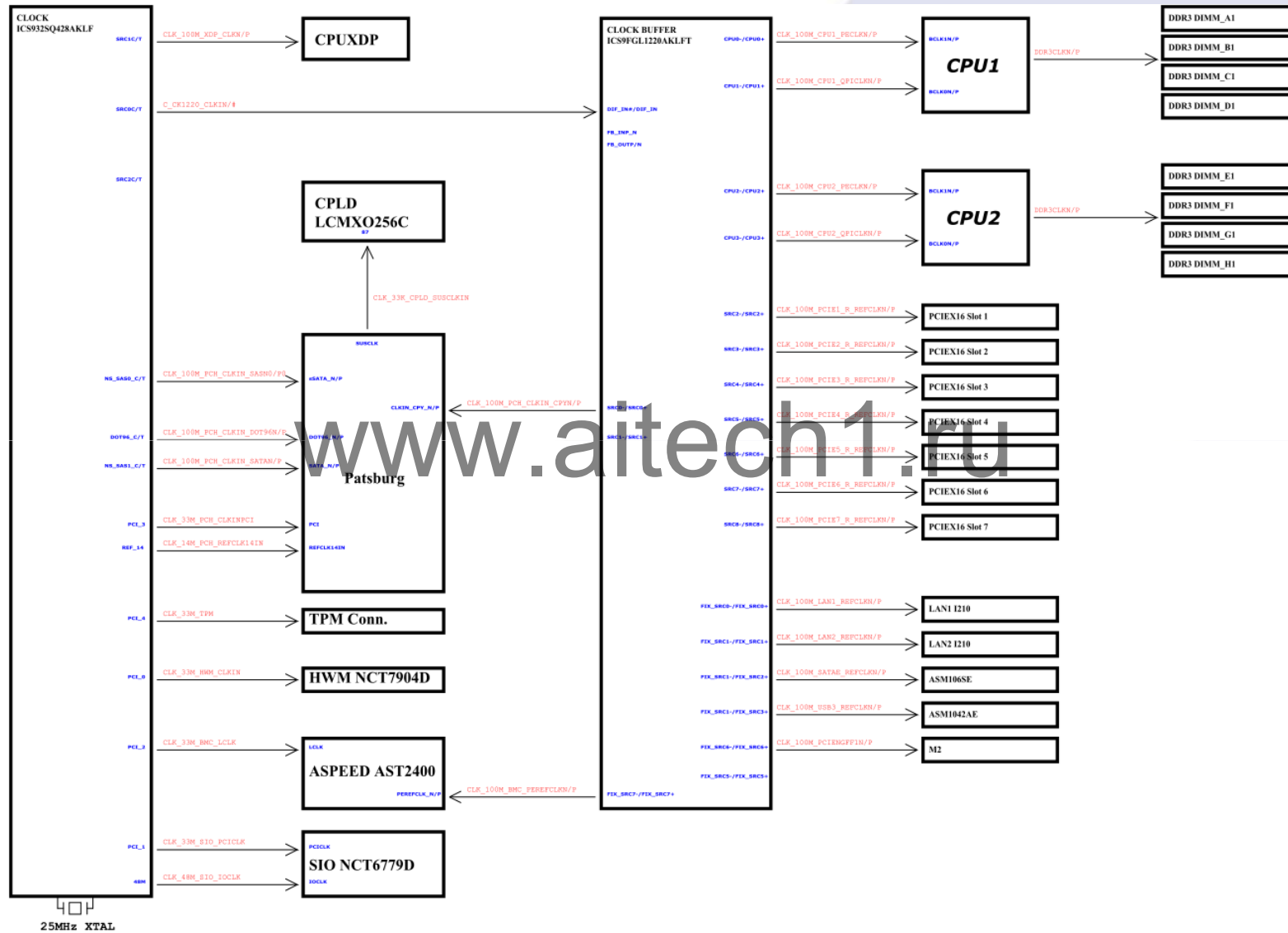
Block Diagram



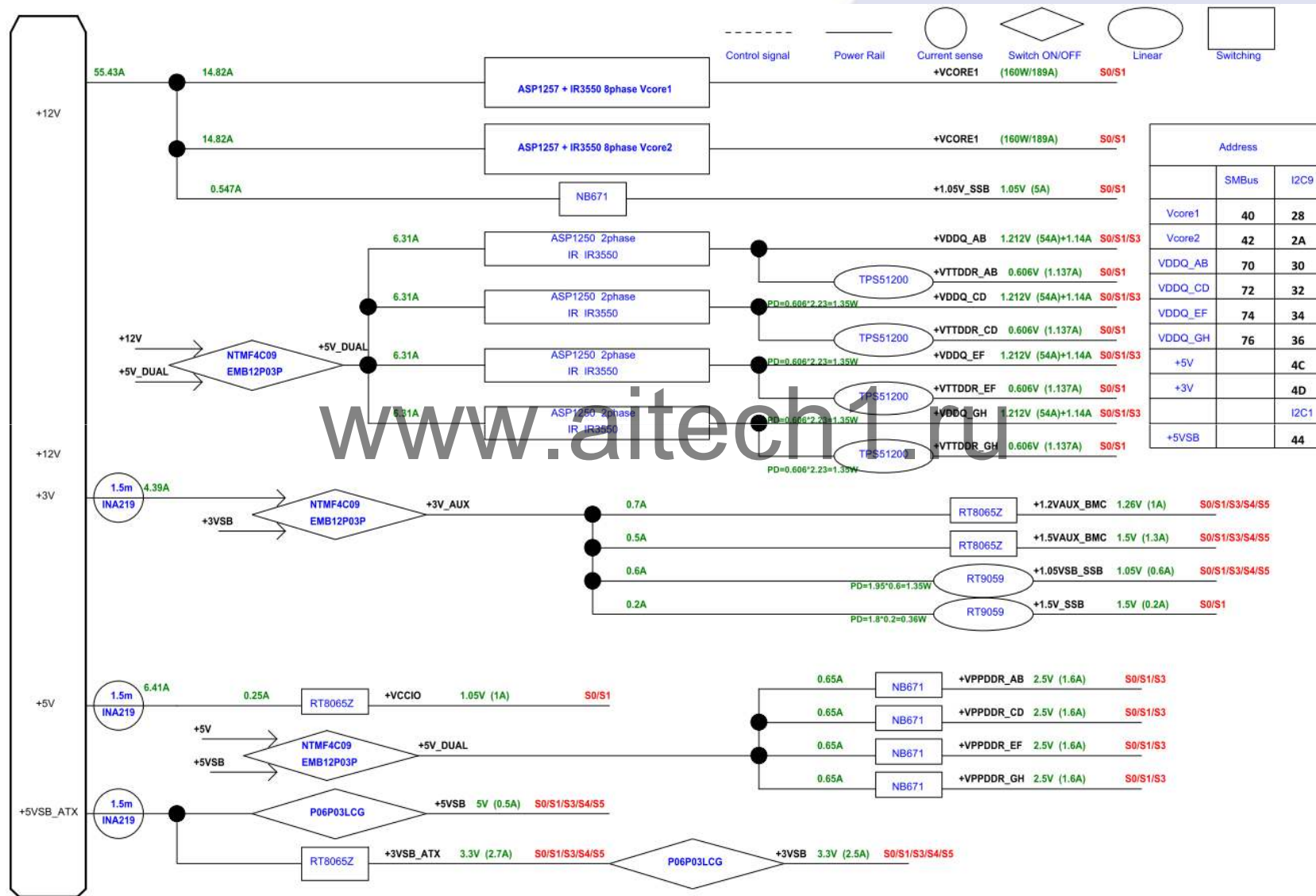
Power Sequence

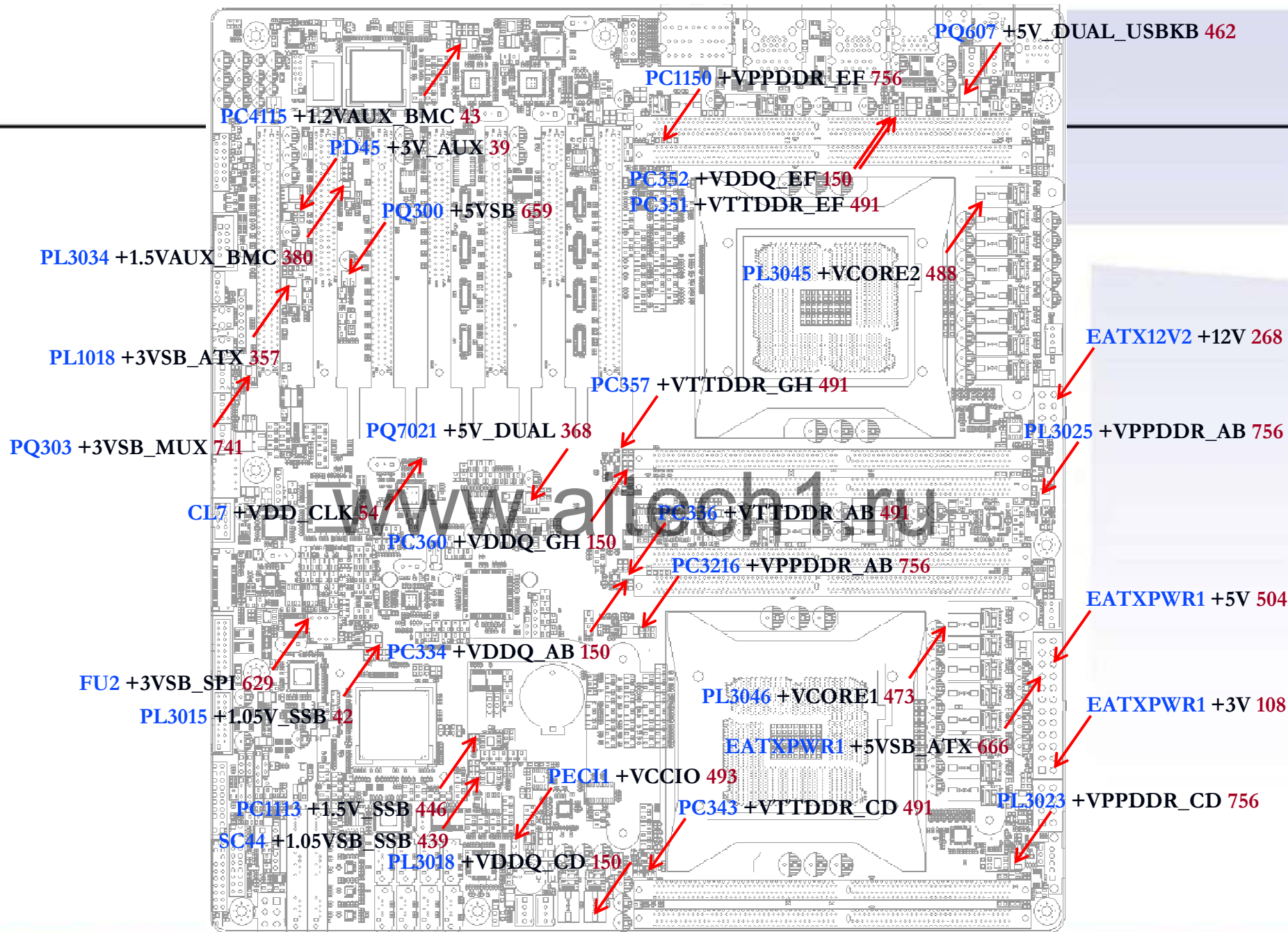
1. VBAT 1 -> 2 : > 9 ms (t200: Grantley Platform Reset and Power Sequencing-513424 r1.1 / P.10)	18. PCH_SUSWARN# 18 -> 19 : = 220 ms (RC delay, not define in datasheet)	32. ATXPGD 32 -> 33 : > 0 ms (NCT6779D r0.6 / P.34)	47. +VTTDDR_AB/CD/EF/GH
2. PCH_RTCRST#	19. PCH_SUSACK#	32 -> 36 : = 0 ms (not define in datasheet)	48. CPLD_CLKEN 48 -> 52 : > 1 ms (t208: Grantley Platform Reset and Power Sequencing-513424 r1.1 / P.10)
3. CPU1_SKTOCC#/CPU2_SKTOCC#	20. PCH_SLPA# 20 -> 21 : = 4 ms (RT9059-DS9059-P01 / P.7)	33. SIO_PWROK 33 -> 34 : > 0 ms (MOS delay, not define in datasheet)	49. CPLD_VCORE1/2_EN 49 -> 50 : < 5 ms (t304: Grantley Platform Reset and Power Sequencing-513424 r1.1 / P.10)
4. Power Plug	21. +1.05VSB_SSB 21 -> 22 : = 200 us (RT9059-DS9059-P01 / P.7)	34. +3V_AUX(MAIN)	50. +VCORE1/+VCORE2 50 -> 51 : < 100 us (t306: Grantley Platform Reset and Power Sequencing-513424 r1.1 / P.10)
5. +5VSB_ATX	22. +1.05VSB_SSB_PWR0K 22 -> 23 : > 1 ms (Mayan city CHB fab3 / P.12) (t207: Grantley Platform Reset and Power Sequencing-513424 r1.1 / P.10)	35. SPI_STRAP	51. +VCORE1/2_PWRGD 51 -> 52 : > 0 ms
5. +5V_DUAL_USBKB(ATX)	23. CPLD_APWROK	36. FM_VCC_MAIN_EN 36 -> 37 : = 0 ms (PATH2: Default Unmount) (RT8065 / P.8)	52. CPLD_PCH_PWROK (CPLD_PCH_PWROK = +1.5V_SSB_PWRGD & 100ms & +VDDQ_PWRGD) 52 -> 53 : > 0 ms
6. +3VSB_ATX 6 -> 7 : = 250 us 6 -> 8 : = 10 ms (t200b: Grantley Platform Reset and Power Sequencing-513424 r1.1 / P.10)	24. R_FP_PWRBNT# 24 -> 25 : = 64 ms (T1: NCT6779D r0.6 / P.259)	37. +VCCIO 37 -> 41 : = 1 ms (RT8065 / P.8)	53. CPLD_SYS_PWROK (CPLD_SYS_PWROK = CPLD_PCH_PWROK & +VCORE_PWRGD) 53 -> 54 : > 1 ms (t206: Grantley Platform Reset and Power Sequencing-513424 r1.1 / P.10)
7. +3VSB_ATX_PWROK	25. SIO_PSOUT# 25 -> 26 : > 0 ms (not define in datasheet)	38. +1.05V_SSB 38 -> 39 : = 1 ms (NB671 / P.7)	54. PCH_DRAMPWROK 54 -> 55 : > 1 ms (t209: Grantley Platform Reset and Power Sequencing-513424 r1.1 / P.10)
8. PCH_DPWROK 8 -> 9 : > 95 ms (t202: Grantley Platform Reset and Power Sequencing-513424 r1.1 / P.10)	26. PCH_SLPS# 26 -> 27 : > 0 ms (t205: Grantley Platform Reset and Power Sequencing-513424 r1.1 / P.10)	39. +1.05V_SSB_PG_20 (RT9059 / P.7)	55. PCH_PROCPWROK 55 -> 56 : = 0 ms
9. PCH_SLPSUS# 9 -> 10 : > 0 ms (MOS delay, not define in datasheet)	27. PCH_SLPS4# 27 -> 28 : > 30 us (t204: Grantley Platform Reset and Power Sequencing-513424 r1.1 / P.10)	40. +1.5V_SSB 40 -> 41 : = 200 us (RT9059 / P.7)	56. CPLD_CPU1/2_PWRGOOD 56 -> 57 : > 0 ms (BJT delay)
10. +5VSB/+3VSB	28. PCH_SLPS3#	41. +1.5V_SSB_PWRGD	57. LVCL_CPU1/2_PWRGOOD 57 -> 58 : > 5 ms (t309: Grantley Platform Reset and Power Sequencing-513424 r1.1 / P.10)
11. +3V_AUX(VSB)	29. SIO_PSON# CPLD_PSON 29 -> 30 : > 0 ms (MOS delay, not define in datasheet)	42. CPLD_DDR_CPU1_EN CPLD_DDR_CPU2_EN 42 -> 43 : = 1 ms (PATH2: Default Unmount) (NB671 / P.7)	58. PCH_PLTRST#
10 -> 11 : = 250 us (RT8065ZQW / P.8)	30. ATXPSON# BMC_ATXPSON#	43. +VPPDDR_AB/CD/EF/GH 43 -> 44 : = 1 ms (NB671 / P.7)	
11. +1.5VAUX_BMC 11 -> 12 : = 250 us	31. +3V/+5V/+12V/-12V +12VSB_NVDIMM/+5V_DUAL 31 -> 32 : 100 ~ 500 ms (T3: ATX DG P.19) (t18: Romley Platform Reset and Power Sequencing-443914 r0.95 / P.15)	44. +VPPDDR_AB/CD/EF/GH_PWRGD 44 -> 45 : > 0 ms (t301: Grantley Platform Reset and Power Sequencing-513424 r1.1 / P.10)	
12. +1.5VAUX_BMC_PWRGD 12 -> 13 : = 750 us (RT8065ZQW / P.8)	31 -> 33 : 300 ms (NCT6779D r0.6 / P.34)	45. +VDDQ_AB/CD/EF/GH 45 -> 46 : < 100 us (t302: Grantley Platform Reset and Power Sequencing-513424 r1.1 / P.10)	
13. +1.2VAUX_BMC 13 -> 14 : = 250 us	31 -> 33 : 300 ~ 500 ms (t2: NCT6779D r0.6 / P.46)	46. +VDDQ_AB/CD/EF/GH_PWRGD 46 -> 47 : > 0 ms (t303: Grantley Platform Reset and Power Sequencing-513424 r1.1 / P.10)	
14. +1.2VAUX_BMC_PWR0K 14 -> 15 : > 0 ms (MOS delay, not define in datasheet)	31 -> 37 : > 0 ms (PATH1: Default Mount)		
15. BMC_DDR3_RESET# BMC_RESET# 6 -> 16 : = 250 ms (NCT6779D r0.6 / P.29)	31 -> 38 : > 0 ms (PATH1: Default Mount)		
16. R_SIO_RSMRST# 16 -> 17 : = 5 ms (t202a: Grantley Platform Reset and Power Sequencing-513424 r1.1 / P.10)	31 -> 43 : > 0 ms (PATH1: Default Mount)		
16 -> 20 : > 100 ms (t12: Romley Platform Reset and Power Sequencing-443914 r0.95 / P.15)			
17. CLK_33K_CPLD_SUSCLKIN 17 -> 18 : > 0 ms (not define in datasheet)			

Clock Distribution



Power Flow





PQ23 +3VSB_ATX_PWROK 992

PR620 SIO_PWROK 8

HR425 CPLD_CPU2_PWRGOOD 904

PR616 PCH_SLPS3# 304

D5 CPLD_PSON ∞
U11 SIO_PWROK 9

PR3239 +VPPDDR_GH_PWRGD 899

PR992 +VPPDDR_AB_PWRGD 899

O3Q1 PCH_SLPSUS# 309

Q41 SIO_PSON# ∞
U6 CPLD_CPU1_PWRGOOD 904

R13 CPLD_DDR_CPU2_EN ∞

PR3245 +1.5V_SSB_PWRGD ∞

PR3242 CPLD_DDR_CPU1_EN ∞

PR3242 CPLD_DDR_CPU1_EN ∞

OQ45 R_SIO_RSMRST# 8

U6 PCH_PROCPWRGD 957

U6 CPLD_SYS_PWROK 739

HR17 PCH_DRAMPWROK 280

EATXPWR1 ATXPSON# 505

PR3252 +1.05V_SSB_PG 20 ∞

PR1160 PCH_SLPA# 302

Q30 CPLD_PCH_PWROK ∞

PR3226 +VPPDDR_CD_PWRGD 899

CLRTC1 PCH_RTCRST# ∞

SQ8 PCH_SLP4# 308

PQ7030 ATXPGD 759

